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Attorney's Docket No.: 10559-606001 / P12890

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler et al.   Art Unit   : Unknown
Serial No. : 10/007,007   Examiner : Unknown
Filed   : December 4, 2001
Title   : PROVIDING MODELING INSTRUMENTATION WITH AN APPLICATION
             PROGRAMMING INTERFACE TO A GUI APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

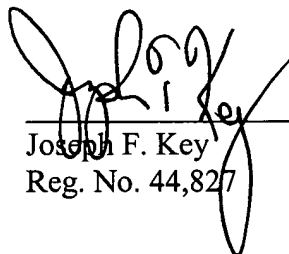### INFORMATION DISCLOSURE STATEMENT

Copies of the references listed on the attached form PTO-1449 are enclosed.

This statement is being filed before the receipt of a first Office action on the merits.

Please apply any charges or credits to Deposit Account No. 06-1050.
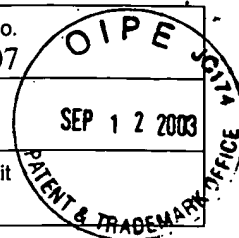
Respectfully submitted,

Date: 9/12/2003

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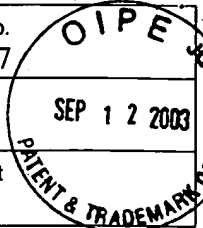Telephone: (202) 783-5070
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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-606001	Application No. 10/007,007
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant William R. Wheeler et al.	
(37 CFR §1.98(b))		Filing Date December 4, 2001	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	5,598,347	01/28/1997	Iwasaki			
	AB	RE 38,059	04/01/2003	Yano et al.			
	AC	6,574,787	06/03/2003	Anderson			
	AD	6,539,536	03/25/2003	Singh et al.			
	AE	6,523,156	02/18/2003	Cirit			
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	AZ	4,703,435	10/27/1987	Darringer et al.			
	AAA						

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		Filing Date December 4, 2001	Group Art Unit

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	ABB	JP 2001068994	03/16/2001	Japan	RECEIVED		Abstract only	
	ACC	EP 720233	07/03/1996	European Patent	SEP 1 6	2003	X	
	ADD	JP 07049890	02/21/1995	Japan	Technology Center 2100		Abstract only	
	AEE	JP 58060559	04/11/1983	Japan			Abstract only	
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Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AGG	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345 (7pages)
	AHH	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, 17 September 2000, pp. 487-493.
	AII	
	AJJ	

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Substitute Disclosure Form (PTO-1449)